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(54) Methods for preventing disturbance of antifuses during programming.

(57) A method to minimize disturbance of an already programmed antifuse while programming other antifuses in a circuit includes the steps of determining a preferred order in which to program the antifuses and programming them in the preferred order. High initial programming and soak currents are selected such that the disturb current is small with respect thereto. The magnitude of the disturb current is increased to a value that maintains the antifuse resistance or improves it rather than adversely affect it. Where a circuit node containing a first already programmed antifuse is positioned such that parasitic capacitances may discharge through that antifuse during the programming of a second antifuse, the magnitude of the charge stored at parasitic capacitances associated with the programming path is reduced by reducing the programming voltage when this programming situation is detected. After the initial rupturing of the antifuse dielectric is detected, the programming voltage is increased to its normal value for the soaking period.

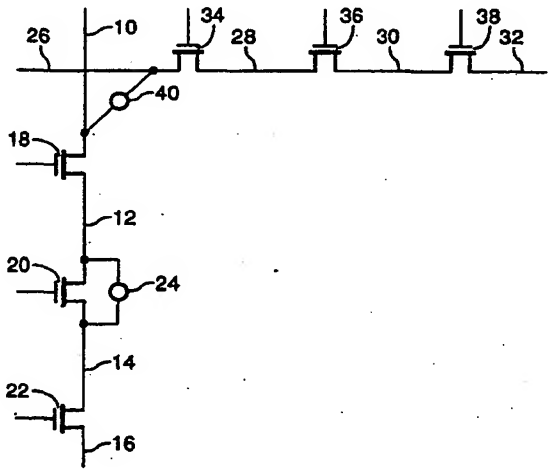

FIG. 1

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BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to user programmable circuits. More specifically, the present invention relates to antifuse elements for use in such circuits and to methods for programming such antifuse elements. In particular, the present invention relates to methods for minimizing the disturbance to already programmed antifuses caused by subsequent programming of other antifuses.

2. The Prior Art

Antifuses, such as those disclosed in United States Patents Nos. 4,823,181 and 4,899,205 are programmed using known methods. In addition, such antifuses disposed in circuit architectures such as disclosed in United States Patent No. 4,758,745 may be programmed by known methods. Co-pending application serial no. 381,630, filed July 19, 1989 and co-pending application entitled Method of Reducing Antifuse Resistance During Programming, Docket No. 190/89, filed May 16, 1990, commonly owned with the instant application, disclose methods for programming such antifuses in such circuit architectures. These applications and patents are hereby incorporated by reference as if fully set forth.

The process of programming a given one of a plurality of antifuses within a single integrated circuit may "disturb" one or more previously programmed antifuses in the same circuit, i.e., affect the previously-programmed antifuse or antifuses in a manner which raises their on resistance. The effect of raising on resistance of antifuses by disturbing one or more antifuses in a circuit while programming others may seriously degrade the performance of the circuit of which the disturbed antifuse is a part.

An object of the invention is to eliminate or reduce the adverse effects of disturb cycles in antifuse programming sequence. The techniques of the present invention may be used in programming antifuses in a field programmable gate array (FPGA) architecture.

BRIEF DESCRIPTION OF THE INVENTION

In a first aspect of the present invention, a method to minimize disturbance of an already programmed antifuse while programming other antifuses in a circuit includes the steps of determining a preferred order in which to program the antifuses and programming them in the preferred order.

In a second aspect of the present invention, high initial programming and soak currents are selected such that the disturb current is small with respect thereto. By using higher soaking currents, it is assured that the disturb current is small with respect to the soak current and the amount of disturbance is minimized.

In a third aspect of the present invention, the magnitude of the disturb current is increased to a value that maintains the antifuse resistance or improves it rather than adversely affect it. This may be accomplished by turning off the transistor shunting the antifuse.

In a fourth aspect of the present invention, where a circuit node containing a first already programmed antifuse is positioned such that parasitic capacitances may discharge through that antifuse during the programming of a second antifuse, the magnitude of the charge stored at parasitic capacitances associated with the programming path is reduced by reducing the programming voltage when this programming situation is detected. This results in a much lower charge and therefore a smaller AC disturb current. The reduction in programming voltage is chosen so that the resulting AC disturb current is negligible and has no effect on the antifuse resistance. After the initial rupturing of the antifuse dielectric is detected, the programming voltage is increased to its normal value for the soaking period.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a typical circuit containing several antifuses and shunting series pass transistors illustrating one aspect of the present invention.

FIG. 2 is a schematic diagram of a typical circuit containing several antifuses and shunting series pass transistors illustrating a second aspect of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Antifuses are programmed by application of a high voltage across their two terminals. The programming voltage (V_{PP}) which may be used is typically 18 volts. After the antifuse dielectric ruptures, a conductive filament having a finite resistance is established between its two terminals. The antifuse may then be soaked with current for a period of time to optimize the resistance of the antifuse. Soak currents may typically be in the range of 3-15 mA.

Antifuses which are programmed with lower programming and soak current have a tendency to exhibit poor (i.e., high) final antifuse resistance. A main reason for the poor resistance is that subsequent programming cycles in the FPGA, intended

for programming other antifuses, produce currents which disturb the earlier antifuses. These subsequent programming cycles will be referred to herein as "disturb cycles." Methods for minimizing the effects of these disturb cycles are the subject matter of the present invention.

The antifuse disturb phenomena can be best understood by first referring to FIG. 1, which illustrates in schematic form a typical circuit containing several antifuses and shunting series pass transistors. FIG. 1 illustrates a plurality of vertical wiring segments 10, 12, 14, and 16 joined together by series pass transistors 18, 20 and 22. Antifuse 24 shunts series pass transistor 20. A plurality of horizontal wiring segments 26, 28, 30, and 32 are joined together by series pass transistors 34, 36 and 38. A second antifuse 40 is connected between vertical segment 10 and horizontal segment 26.

In order to program antifuse 24, a source of programming voltage V_{PP} is applied to segment 10 (or segment 16) and ground is applied to segment 16 (or segment 10). Transistor 20 is connected in parallel with antifuse 24 so its gate is turned off. Transistors 18 and 22 have their gates turned on by connecting them to V_{PP}. The circuit thus applies the V_{PP} voltage across one terminal of antifuse 18 and ground to the other terminal as disclosed in U.S. Patent 4,758,745. After a short period of time, typically a few milliseconds, the antifuse programs and a resistance is established between its terminals. The antifuse may then be current soaked for a period of time (as described in co-pending application entitled Method of Reducing Antifuse Resistance During Programming, Docket No. 190/89, filed May 16, 1990) to optimize the final antifuse resistance.

One type of disturb cycle referred to herein occurs while subsequently programming antifuse 40 after antifuse 24 has been programmed. V_{PP} is applied to the terminals of antifuse 40 again by supplying V_{PP} from one side through transistors 18, 20 and 22 while supplying ground through transistors 34, 36, and 38 as explained in U.S. Patent 4,758,745. The gates of all transistors in this programming path are turned on with V_{PP}. Antifuse 40 programs the same way as did antifuse 24 and a resistance is established between its terminals.

During the current soaking cycle a current is passed through antifuse 40. As can be seen from FIG. 1, the soaking current travels through two parallel paths, programmed antifuse 24 and transistor 20. Because of the current passing through programmed antifuse 24, this programming cycle for antifuse 40 is referred to as a disturb cycle for antifuse 24 with the current through antifuse 24 as the disturb current.

Since the soaking curr nt is divided between transistor 20 and already programmed antifuse 24, the disturb current may be relatively small if it is assumed that the on resistance of transistor 20 is lower than the programmed resistance of antifuse 24. If the disturb current is 1-3 Ma and antifuse 24 was previously programmed with a similar or slightly larger current than the disturb current, antifuse 24 will be disturbed and may end up with a very poor antifuse resistance value, i.e.,10k-20k ohms.

According to the present invention, a preferred solution to the disturb problem is to modify the antifuse programming order so that antifuse 40 is programmed before antifuse 24. In this case, no disturb current passes through antifuse 24. A subsequent programming cycle would then be used to program antifuse 24. In this instance, no disturb current will pass through antifuse 40 since the programming path does not use transistors 34, 36, and 38.

Another preferred solution to this problem according to the present invention is to design the programming path to deliver high initial programming and soak currents. By using higher soaking currents, it is assured that the disturb current is small with respect to the soak current and the amount of disturbance is minimized.

Another preferred solution according to the present invention for this architecture is to increase the magnitude of the disturb current to a value that maintains the antifuse resistance or improves it rather than adversely affect it. This may be accomplished by turning off transistor 20 so that all of the soaking current for antifuse 40 passes through already programme antifuse 24.

Another type of disturb cycle which may be minimized using the techniques of the present invention will now be described with reference to FIG. 2. Referring now to FIG. 2, plurality of vertical segments 50, 52, 54, 56, and 58, are joined by series pass transistor 60, 62, 64, and 66. Series pass transistor 64 is shunted by anti-fuse 68. A plurality of horizontal wiring segments 70, 72, 74 and 76 are connected by series pass transistor 78, 80 and 82. Anti-fuse 84 is connected between horizontal segments 70 and vertical segment 54. During the programming of anti-fuse 84, the high voltage V_{PP} is propagated from the supply through wiring segments 50 and 52 and transistors 60 and 62 to the side of antifuse 84 connected to wiring segment 54. The other side of antifuse 84 is returned to ground through wiring segments 72, 74, and 76 and transistors 78, 80 and 82. If antifuse 68 has been previously programmed, the programming voltage V_{PP} is also propagated to its other end and to wiring segment 56.

At this point in time, parasitic capacitances 86 and 88 associated with both ends of antifus 68, i.e., the parasitic capacitances shown in phantom

lines associated with wiring segments 54 and 56, ar charged up with a charge equal to the voltage V_{PP} multiplied by the capacitance seen at the respective node (Charge $Q = C * V$). When antifuse 84 initially ruptures, current flows through anti fuse 84 to ground via wiring segments 72, 74, and 76 and transistors 78, 80 and 82 through two paths. The first path is the intended current path current from V_{PP} at wiring segment 50 through transistors 60 and 62 and wiring segments 52 and 54. In addition, however, a second, unintended path exists as a capacitive discharge path for capacitance 86 at wiring segment 54 and capacitance 88 at wiring segment 56 through already programmed antifuse 68. The AC transient caused by this capacitive discharge can be of a magnitude high enough to disturb antifuse 68. As the voltages on wiring segments 54 and 56 decay to the steady state final value, an AC current is drawn through antifuse 68. The magnitude of the AC current is determined by the initial charge stored at parasitic capacitance 88 and the rate of discharge of the circuit which is a function of the circuit. This AC current is a disturb current through previously programmed antifuse 68. It has been observed that this current adversely affects the resistance of antifuse 68.

According to the present invention, a preferred solution to this problem is to reduce the magnitude of the charge stored at parasitic capacitances 86 and 88. This is accomplished by reducing the programming voltage when this programming situation is detected. This results in a much lower charge and therefore a smaller AC disturb current. The reduction in programming voltage is chosen so that the resulting AC disturb current is negligible and has no effect on the antifuse resistance. In a preferred embodiment, a reduction of 2 volts in the programming voltage was sufficient to solve the AC disturb problem. After the initial rupturing of the dielectric of antifuse 84 is detected, V_{PP} is increased to its normal value for the soaking period.

Another solution to this problem would be to modify the programming order of the antifuses whenever possible so that antifuse 84 is programmed prior to antifuse 68. This is not always possible in all architectures.

While presently-preferred embodiments of the invention have been disclosed, those of ordinary skill in the art will, from an examination of the within disclosure and drawings be able to configure other embodiments of the invention. These other embodiments are intended to fall within the scope of the pr sent invention which is to be limited only by the scope of the appended claims.

Claims

1. A method for minimizing disturbance to a first already programmed antifuse caused by the subsequent programming of a second antifuse, including the steps of,

determining a preferred programming order such that programming of said second antifuse will not cause current to flow through said first antifuse,

programming said first and second antifuses in said preferred programming order.

2. A method for minimizing disturbance to a first already programmed antifuse caused by the subsequent programming of a second antifus , including the steps of,

determining a disturb current which will flow through said first antifuse during programming of said second antifuse,

programming said second antifuse using a programming current and a soaking current having magnitudes greater than the magnitude of said disturb current.

3. A method for minimizing disturbance to a first already programmed antifuse caused by the subsequent programming of a second antifuse, said first antifuse shunted by a transistor, including the step of turning off said transistor during the programming of said second antifuse.

4. A method for minimizing disturbance to a first already programmed antifuse caused by th subsequent programming of a second antifuse, said first antifuse located between a first node having a parasitic capacitance and a second node comprising a source of programming voltage having an initial value, said second antifuse located between said second node and a third node comprising a source of ground potential, including the steps of:

determining whether said first antifuse is located between said first node said second node,

determining if said second antifuse is located between said second node and said third node,

reducing the magnitude of said programming voltage from said initial value to a second, lower value if said first and second antifuses are so located,

applying said programming voltage of said second value to said second node,

increasing said programming voltage to said initial value when said antifuse begins to draw current.

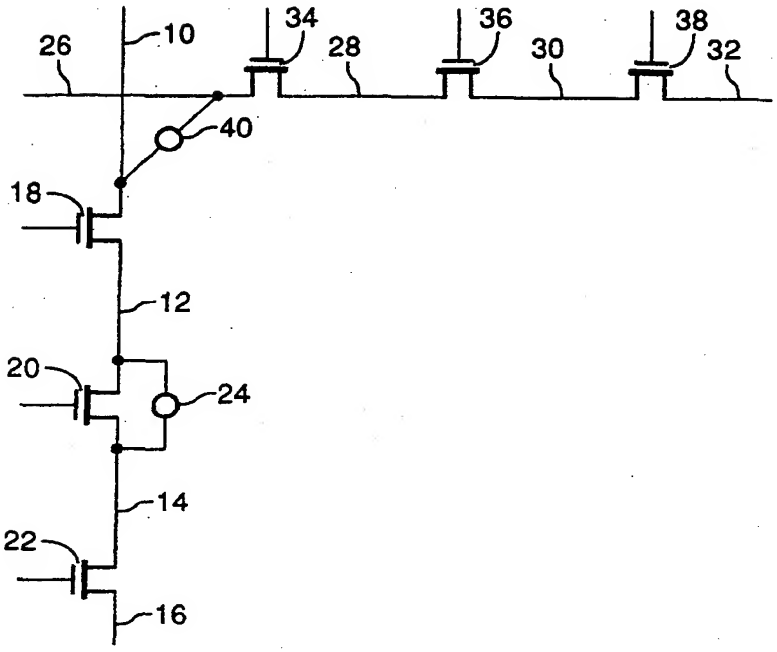

FIG. 1

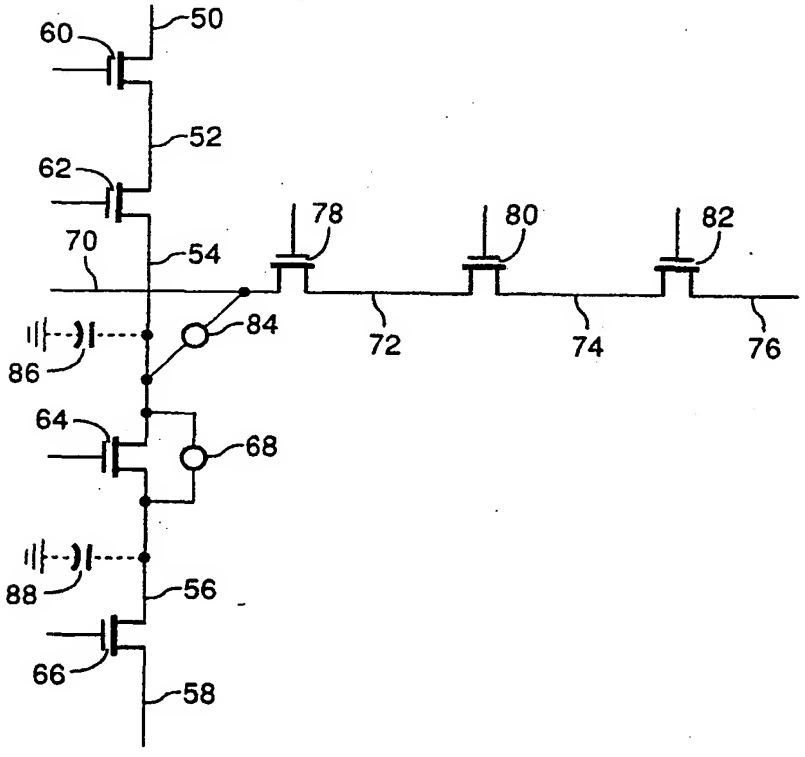

FIG. 2

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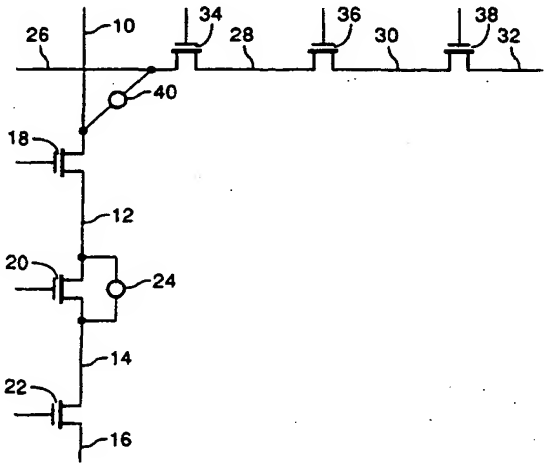

FIG. 1

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EUROPEAN SEARCH REPORT

Application Number

EP 91 30 3915

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X,D	US-A-4 758 745 (ELGAMAL et al.) * Abstract; column 9, line 9 - column 10, line 27; figures 7a-7e *	1	G 11 C 17/18
A,D	---	2-4	
X	PROCEEDINGS OF THE IEEE 1988 CUSTOM INTEGRATED CIRCUITS CONFERENCE, Rochester, NY, 16th - 19th May 1988, pages 1541-1544; A. EL GAMAL et al.: "An architecture for electrically configurable gate arrays" * Whole document *	1	
A	--- IDEM -----	2-4	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
G 11 C 17/18
G 11 C 17/16
H 03 K 19/177

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23-12-1992	STECCHINA A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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